Printed Circuit Board Design Considerations

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Steady advances in IC technology have fueled 30 years of rapid progress in digital system speed and complexity. In the past, system speed was determined by gate and register performance, and you could easily take advantage of ever faster, bigger, and cheaper integrated circuits.

The printed circuit board (PCB) was just a means to hold ICs in place; PCB layout was an exercise in topology and economics. Analog issues such as crosstalk, phase and amplitude distortion, reflections, ground bounce and so on could thus safely be ignored, or treated as minor irritants, because synchronous digital logic is forgiving in amplitude and timing variations.

Times have changed. At today's circuit speed, the PCB and its analog characteristics play a strong, if not dominating, role in determining digital system performance.

CMOS ICs are no longer the slow and forgiving circuits of the past. They are now as fast as (if not faster than) the fastest TTL circuits; outputs ramp between 0 and 5 volts in 1 ns, clock rates approach 150 MHz, and ICs have up to 500 signal connections to accommodate multiple 32-bit wide busses. The trend is moving toward much higher speed and far more I/Os.

However, signals still travel along PCB traces at only half the speed of light, and sharp signal edges get reflected at every trace discontinuity. You must now not only control the source-to-destination path, but you must also pay attention to the complete circuit loop and its inductance, from the positive power supply terminal back to the negative terminal, then through the decoupling capacitors back to the positive supply terminal.

This means that the PCB plays an important role in controlling the integrity of interconnect signals. Trace width and trace spacing as low as 4 mils (0.1 mm), controlled line impedance, and multi-layer boards with clean ground and Vcc planes, are all required to minimize reflections, ground bounce, and crosstalk. Maintaining clock integrity is a big problem.

Year	Max.System Clock	PC-Board Complexity	PC-Board Min.Trace Width	IC Design Rules
1965	1 MHz	1-2 layers	100 mil = 2.5 mm	10µ
1980	10 MHz	2-4 layers	20 mil = 0.5 mm	3µ
1995	100 MHz	4-8 layers	4 mil = 0.1 mm	0.5µ
2010 ?	1000 MHz	8-16 layers	1 mil = 25 µ	0.1µ

Time Domain vs Frequency Domain

Digital designers usually express delays and rise times in the time domain, while analog designers often use the frequency domain to describe circuit and component performance. The frequency domain is more meaningful for analyzing many analog phenomena. For rough estimates, we can easily convert rise and fall times into a frequency spectrum as follows:

There is a knee frequency
$$F = 0.5 \bullet (1/(T_{rise} \text{ or } T_{fall}))$$

For analyzing circuit behavior, it is sufficient to evaluate the frequency response up to the knee frequency, but there is no need to go higher.

For a typical rise time of 2 ns, the knee frequency is 250 MHz. When low-pass circuits are cascaded, the resulting transition time is the square root of the sum of the squared transition times. For example:

➤ A 250 MHz scope with a 250 MHz probe displays a 2 ns rise time as a 3.5 ns rise time ($\sqrt{2^2 + 2^2 + 2^2}$). This is a +75% error.

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➤ A 500 MHz scope with a 500 MHz scope probe displays a 2 ns rise time as a 2.4 ns rise time ($\sqrt{2^2 + 1^2 + 1^2}$). This is only a +20% error.

Beware of slow scopes and slow scope probes.

PCB Characteristics
➤ Min. trace width: typically 10 mil (0.25 mm), down to 4 mil (0.1 mm)
➤ Min. trace pitch: twice trace width
➤ Hole diameter: 20 mil, down to 8 mil (0.5 mm to 0.2 mm). Thin traces and small holes make the board more expensive.
➤ Layer thickness: typically 8 mil (0.2 mm), down to 4 mil (0.1 mm). The dielectric constant ε is 4.5 for typical FR4 PCB material.

Beware of Trace Inductance
A 0.5-inch long, 10-mil wide trace, over an 8-mil thick PCB layer, connected to the underlying ground plane through a 14-mil via at the end, has an inductance of 9 nH. To a 2-ns rise time, this is an impedance of 15 Ω.

Typical Lumped Parameters
➤ **Capacitance** - A narrow trace has a capacitance of 2 pF per inch (0.8 pF per cm). Copper area has 130 pF per square inch (20 pF per cm^2).
  ➤ Ceramic decoupling capacitors have a series resistance of several ohms, and an inductance of 3 to 30 nH. Use several capacitors in parallel to lower the high-frequency impedance.
  ➤ Via capacitance is 0.5 pF (insignificant) but the inductance of >1 nH can be significant for very fast transitions (3 Ω for a 1-ns transition).
➤ **Inductance** - A 1-inch long wire (25 mm) has an inductance of 80 nH, which at 100 MHz means 50 Ω (definitely *not* a short circuit).
➤ **Resistance** - 1/4 W axial resistors have a series inductance of 2.5 nH and a parallel capacitance of ~2 pF. 1/8 W axial resistors have 1 nH and <2 pF.

Transmission Lines
Short connections can be treated as lumped capacitors, but any line with a propagation delay of more than 30% of the signal transition time must be analyzed as a transmission line. With a 3-ns transition time, any line longer than six inches (15 cm) is a transmission line. With a 1-ns transition time, any line longer than two inches (5 cm) is a transmission line.

Characteristic Impedance of a PCB Trace
➤ 50 Ω for outer trace, width = 2x PCB layer thickness (microstrip).
➤ 75 Ω for outer trace, width = 1x PCB layer thickness (microstrip).
➤ 50 Ω for inner trace, width = 0.6x PCB layer thickness (stripline).
➤ 75 Ω for inner trace, width = 0.25x PCB layer thickness (stripline).

Higher characteristic impedances are unrealistic on modern PCBs.

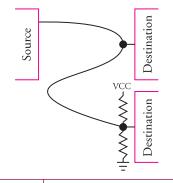## How to Prevent Signal Degradation Due to Reflections (Ringing)
➤ Keep the trace short (best solution, but often impossible).
➤ Terminate at the destination (end termination). *(See Figure1.)*
  Problem: High sink or source current, or both. High power consumption.
  Solution: Capacitive coupling to the terminating resistor. Time constant should be longer than the transition, but much shorter than the flat time. For example: 200 pF x 50 Ω = 10 ns.
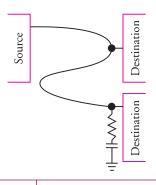 See **Figure 2**.
➤ Terminate at the source (series termination).
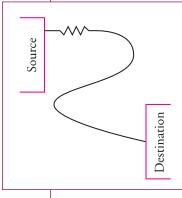 *Advantage*: No static power consumption.

Figure 1.

Figure 2.

Figure 3.

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Problem: Use only for single-destination. 50% amplitude along the trace!
See **Figure 3** .

Signals propagate at the speed of light divided by the square root of the effective dielectric constant. The speed is therefore higher on the outer traces that have air on one side, than on the inner traces that are completely surrounded by epoxy.

➤ Propagation delay on an outer trace: 140 ps per inch (55 ps per cm).
➤ Propagation delay on an inner trace: 180 ps per inch (70 ps per cm).

Ground Plane

Always analyze the whole current loop: Vcc terminal to Vcc distribution, to Vcc-pin, to device output, to PCB trace, to ground distribution, to ground terminal, through the decoupling capacitors, and back to Vcc. Keep this loop inductance as small as possible by reducing the area of the loop. The return current tries to follow the signal trace; it follows the path of least inductance (least energy).

➤ Make it easy for the signal and return paths to stay close together.
➤ Avoid obstacles in the ground plane.
➤ Investigate the reason for any detour of the current.
➤ Watch out for slots in the ground plane causing detours in the return path, leading to crosstalk and ringing.

Ground Bounce

Ground bounce is caused by a voltage drop on the inductance between chip internal ground (bonding wire + leadframe, especially in ceramic PGAs) and PCB ground. The pulse width increases with capacitive loading, but the pulse amplitude is independent of capacitive loading. Ground bounce can cause wrong output levels on adjacent outputs and can cause inputs to be misinterpreted. For a High-to-Low transition, the internal ground jumps first to a positive voltage, then undershoots. *(See the 1998 Xilinx Data Book, pages 13-16)*

Synchronous designs with one common clock are surprisingly resilient. They tolerate ground bounce, because it occurs directly after the triggering clock edge, whereas input levels only matter at setup time before the next active clock edge. However, beware of all asynchronous inputs and clocks — they are susceptible to misinterpretation due to ground bounce. Make sure these signals are parked far away from the input thresholds.

Crosstalk

Crosstalk is especially strong when many lines run closely parallel, as in data busses. Inductive crosstalk is usually bigger than capacitive. Crosstalk can be minimized by using an unobstructed ground plane. Synchronous busses can tolerate a lot of crosstalk if it occurs only after the synchronous data transitions.

Problem: Asynchronous control lines, strobes, interrupts that run parallel to the data or address busses.
Solution: Increase the spacing.

Vcc Decoupling Capacitors

Supply decoupling is not a luxury. For fast internal and external transitions, these capacitors are the only instant source of current. The power supply with its big electrolytic capacitor is too far away and has too much inductance. (See *XCell #20*, pages 42-43). Low-impedance ceramic decoupling capacitors are required to supply dynamically changing Icc inside the chip, and to provide a return path for external current changes. In CMOS systems, all power is dynamic. The instantaneous current peaks are much higher than the average dc current, which is between 100 mA and 2 A for the larger Xilinx devices.

Decoupling capacitors must have low inductance and low series resistance. The capacitance value is irrelevant, as long as it is sufficient. Use 0.01 to 0.1 μF capacitors, mounted very close to each Vcc pin and directly connected to the ground plane. Keep the lines very short. A narrow, 0.25-inch (6 mm) long trace represents 20 nH; a current change of 100 mA/ns causes a voltage drop of 2 volts across this inductance.

Credits

For an excellent, in-depth treatment of these subjects, read "High-Speed Digital Design" by Johnson and Graham, Prentice Hall, 1993, or attend a class given by the author, Howard W. Johnson, Redmond WA. (howiej@olympic-tech.com). ◆